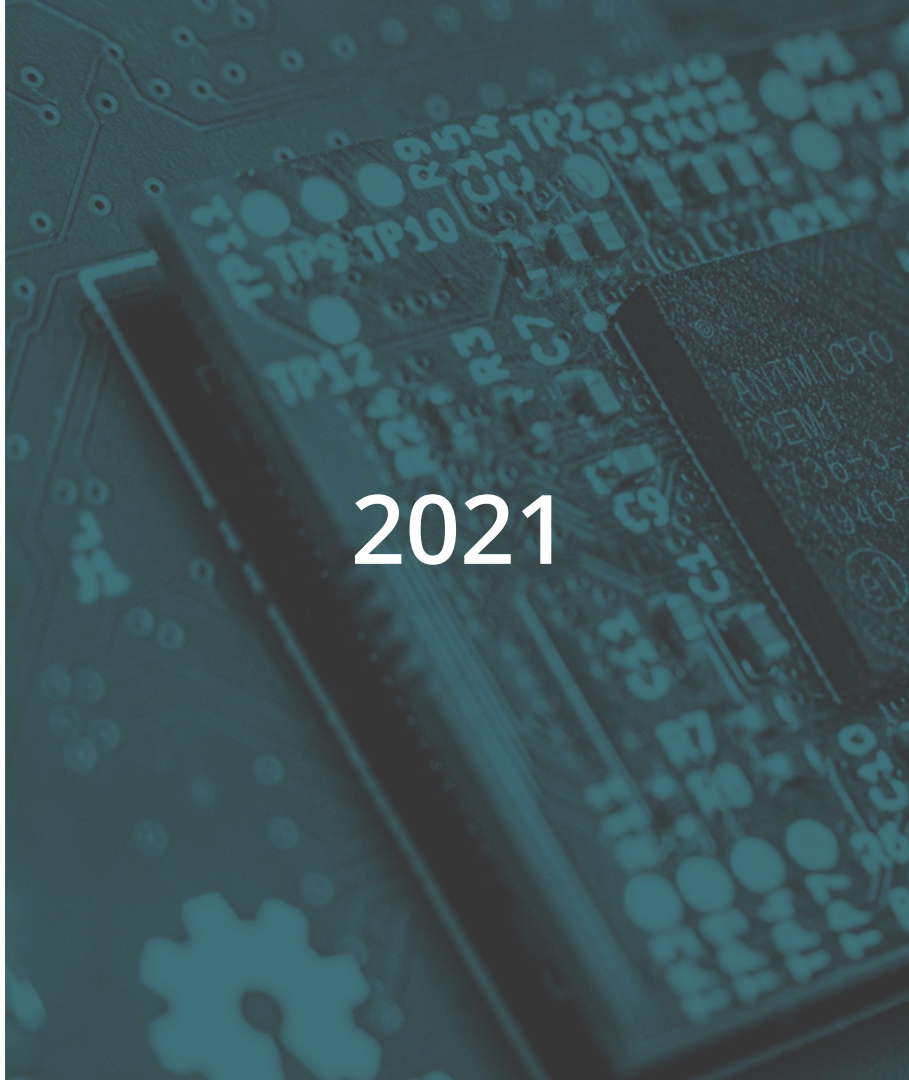
OSSNA 2022 RISC-V BoF

Stephano Cetola
Director of Technical Programs - RISC-V


@risc_v

Where We've Been

- 16 Specs Ratified
  - 44 Extensions Total
- 46 Working Groups
  - 10 Committees
  - 17 SIGs
  - 19 Task Groups



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2022

- 4 Specs Ratified
  - Efficient Trace (E-Trace)
  - Supervisor Binary Interface (SBI)
  - UEFI Protocol
  - Multiply without Divide (Zmmul)
- New Working Groups
  - Floating Point SIG
  - Vector SIG
  - Control Flow Integrity (CFI) TG
  - Universal Discovery TG
  - …

What Comes Next?

The Road Ahead

- Profiles
- Platforms
- SEE
- Unified Discovery
- Debug
- Advanced Interrupts
- Packed SIMD

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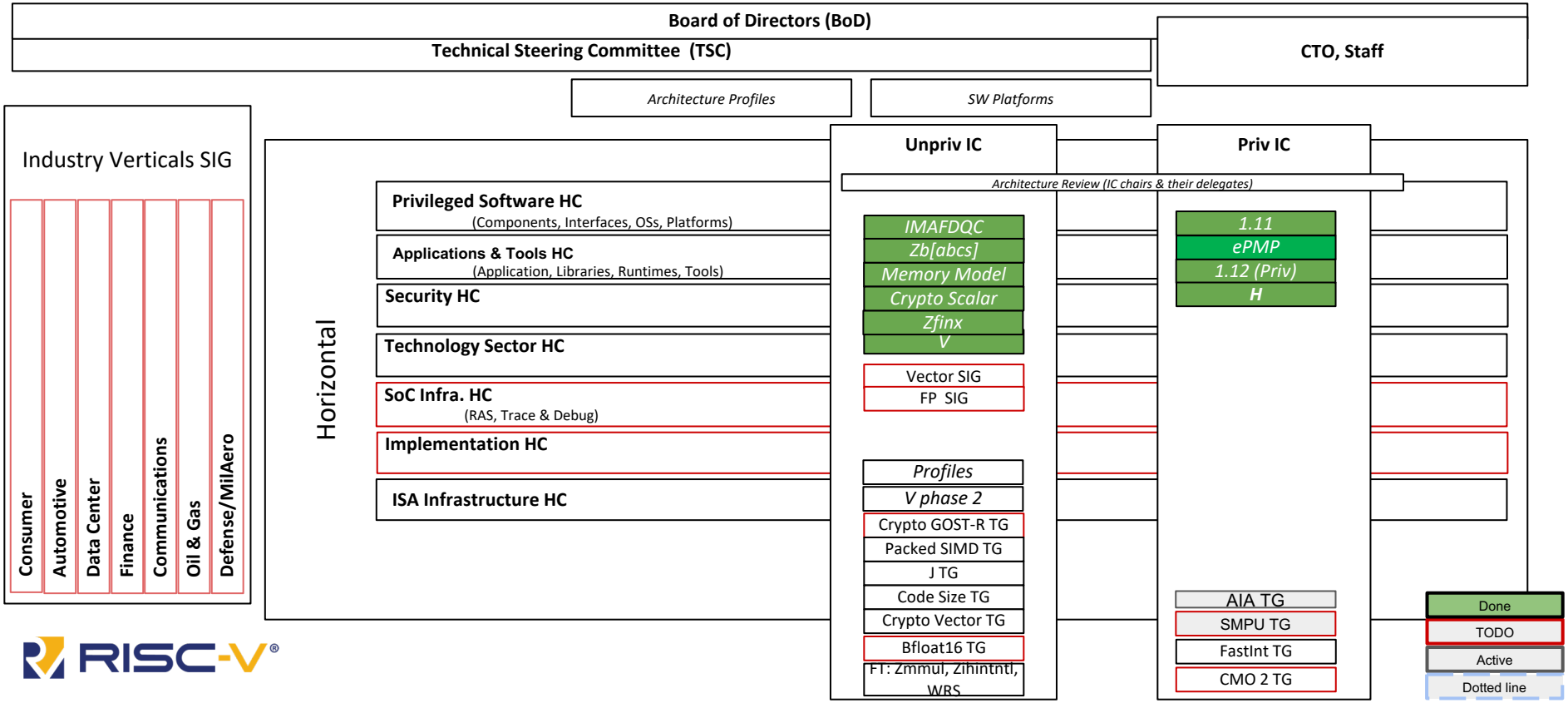
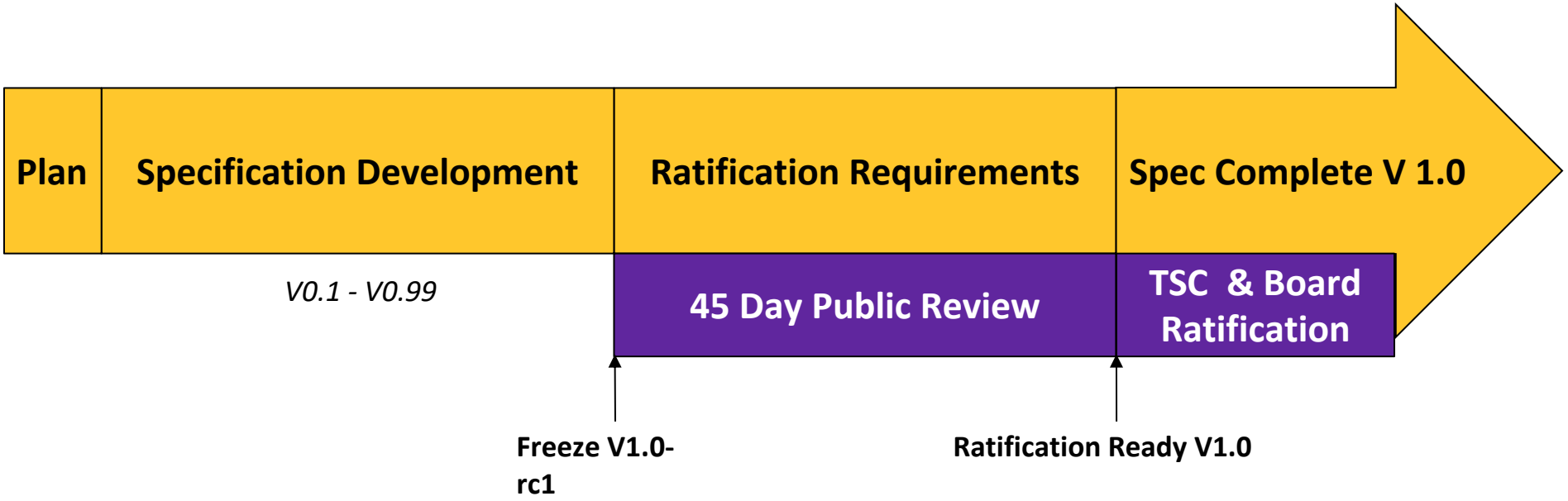
- Total Store Ordering
- Counters (Zicntr, Zihpm)
- Code Size Reduction
- Vector Half Width (Zvfh)
- Bfloat16
- Crypto Vector
- Fast Interrupts
- IOMMU
- IOPMP

How Do We Get There?

Technical Organization

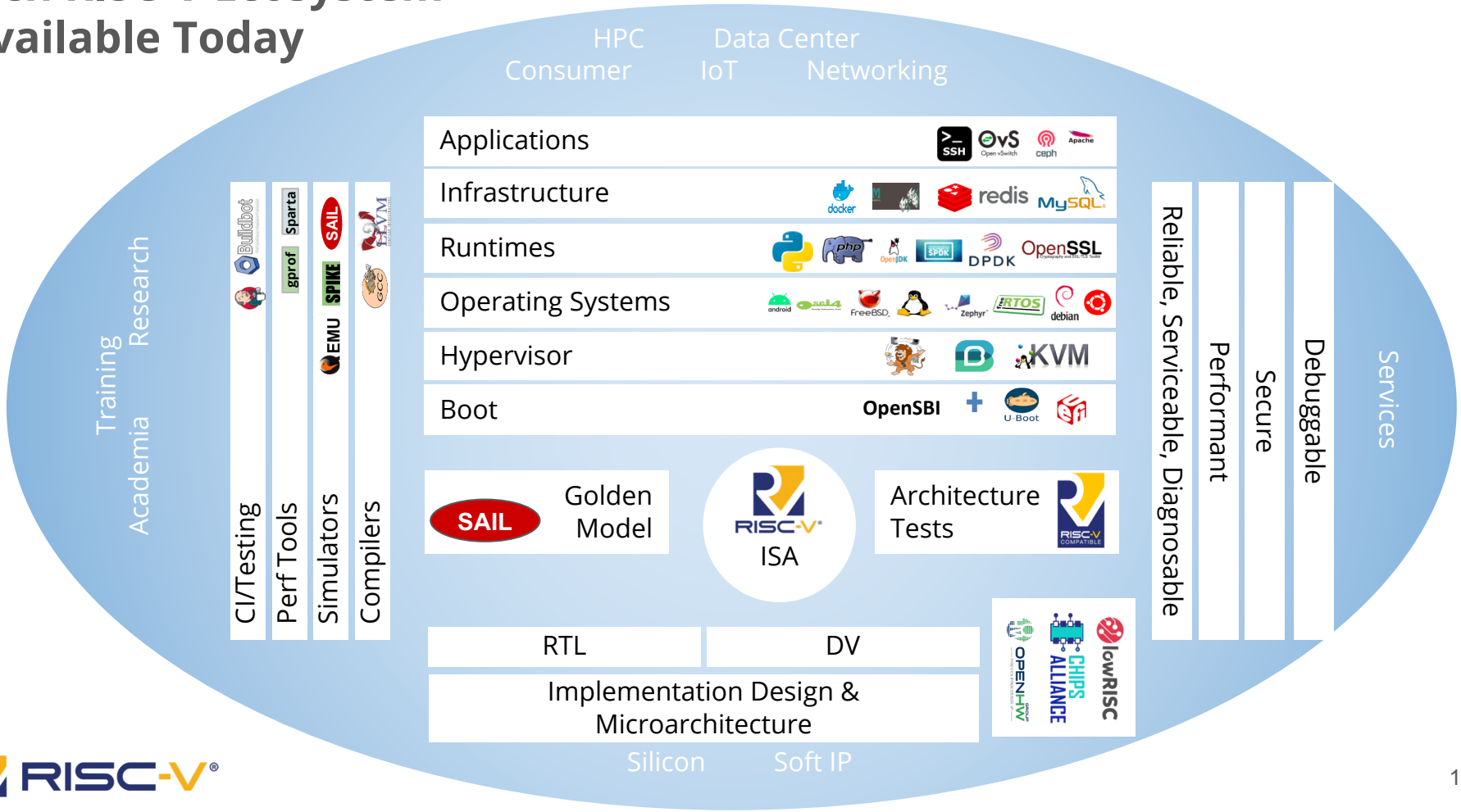


Simplified Specification Lifecycle

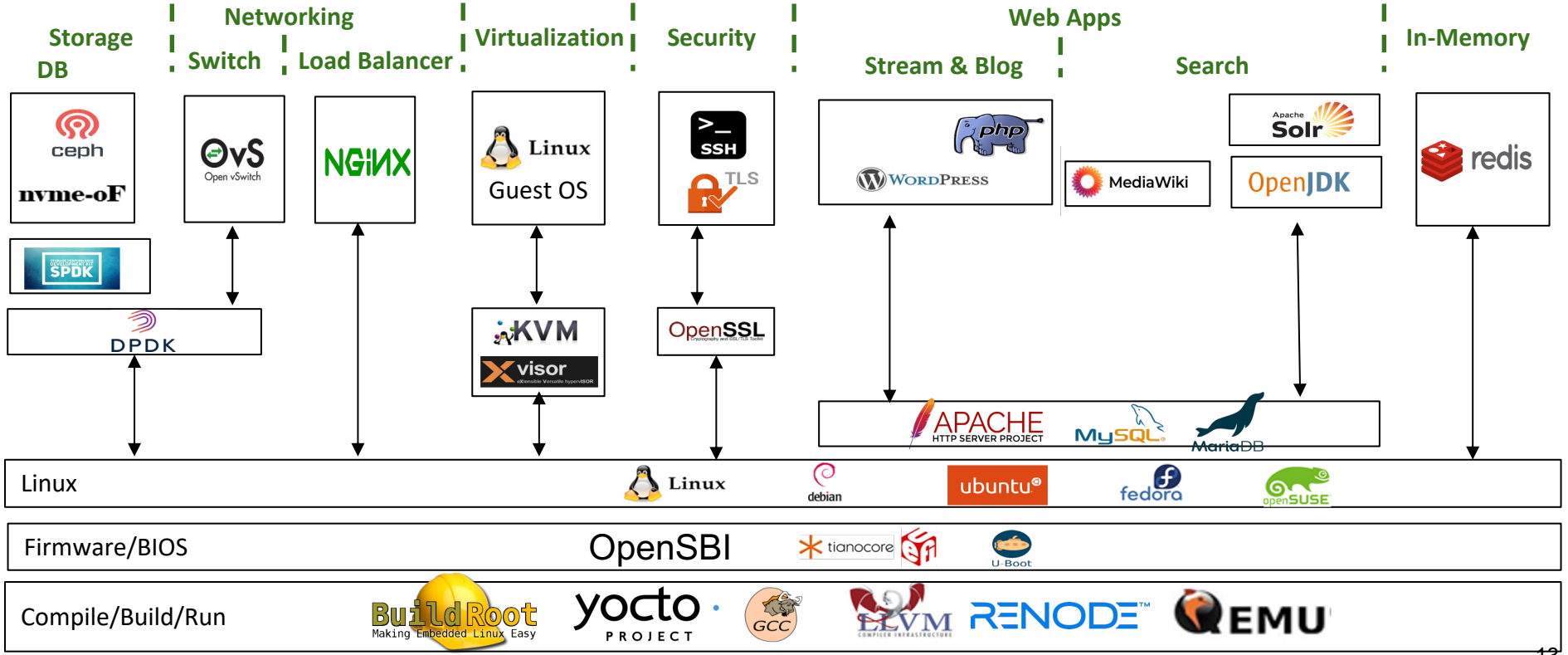


What About Software?

Rich RISC-V Ecosystem Available Today



Software Stack Examples Available Today



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RISC-V Technical Community

- **RISC-V Wiki**
  https://wiki.riscv.org
- **GitHub**
  https://github.com/riscv
- **Member Mailing Lists**
  https://lists.riscv.org
- **Public Mailing Lists**
  Google Groups ➤
  ISA-DEV, HW-DEV, SW-DEV